~~124~~ 119. The semiconductor memory device according to claim ~~115~~ 111 wherein each distance between the first and second impurity regions and between the first and third impurity regions is 0.1 to 0.3 μm.

~~126~~ 131. The semiconductor memory device according to claim 121 ~~126~~ wherein each distance between the first and second impurity regions and between the first and third impurity regions is 0.1 to 0.3 μm.

~~141~~ 139 142. The semiconductor memory device according to claim 121 ~~138~~ wherein each distance between the first and second impurity regions and between the first and third impurity regions is 0.1 to 0.3 μm.

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~~145~~ 120. The semiconductor memory device according to claim 111 ~~145~~ wherein a side edge of said first floating gate is aligned with a side edge of said first control gate, and a side edge of the second floating gate is aligned with a side edge of the second control gate.

Cont'd

~~137~~ 132. The semiconductor memory device according to claim 121 ~~126~~ wherein a side edge of said first floating gate is aligned with a side edge of said first control gate, and a side edge of the second floating gate is aligned with a side edge of the second control gate.

~~144~~ 143. The semiconductor memory device according to claim 133 ~~138~~ wherein a side edge of said first floating gate is aligned with a side edge of said first control gate, and a side edge of the second floating gate is aligned with a side edge of the second control gate.--

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REMARKS

The attached amendment supplements applicant's response filed February 29, 2000 in the above-identified matter. Specifically, the attached supplemental amendment adds new claims 17-154 to complete the scope of protection to which applicant is entitled. These new claims are directed to a second embodiment of the present invention shown in Figures 9A-9E and described beginning on page 17 of the specification. It is noted that

the first impurity region recited in claims 17-111 can be seen in Figure 9 as region 755 which forms a part of both the first and second memories recited in these claims.

New claims 112-154 are similar to claims 17-111 in scope, but recite first and third impurity regions that are formed in a common impurity region of the semiconductor substrate. That is, while a single region 755 is shown in Figure 9, this region corresponds to the recited common impurity region 755 while the first and third impurity regions are intended to refer to only a portion of this region.

Also, applicant again directs the Examiner's attention to Japanese Patent Documents 55-15869 and 52-23532 filed in the Information Disclosure Statement mailed December 21, 1999. In that Applicant has not received an initialed copy of the PTO Form 1449 evidencing consideration of these references, it is requested that the undersigned be contacted if these references have been misplaced or otherwise not made of record in this application.

Entry of this supplemental amendment and favorable action on these new claims is respectfully requested together with consideration of applicant's earlier response.

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285

Nixon Peabody LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110